WHAT IS CLAIMED IS:

1. A method for demodulation of a composite signal containing a plurality of multi-path components, the method comprising:

buffering digital samples of a signal into a first memory element;

randomly accessing the digital samples from the first memory element to correlate a particular multi-path component from the signal; and

iteratively accumulating the correlated particular multi-path component into a second memory element.

2. The method of claim 1, wherein randomly accessing the digital samples from the first memory element to correlate a particular multi-path component comprises accessing digital samples according to paths corresponding to the digital samples.

3. The method of claim 1, wherein iteratively accumulating the correlated particular multi-path component into a second memory element defines a demodulation operation and comprises using information from the signal to determine an amount of demodulation processing to be performed.

4. The method of claim 1, where the determination of multi-path components to be iteratively processed varies dynamically between processing units.

5. The method of claim 1, further comprising performing channel estimation and demodulation via the non-sequential access of digital samples form the first memory element.

6. The method of claim 1, further comprising:

tuning to a non-original RF frequency;

buffering digital samples obtained while tuned at the non-original RF frequency;

retuning the RF frequency to the original frequency; and

performing searching and channel estimation via the random access of the digital samples stored in the first memory element while simultaneously operating on the digital samples of the original frequency.

7. An apparatus configured to demodulate a composite signal containing a plurality of multi-path components, the apparatus comprising:

buffers configured to be switchable between a write state with digital samples and a read state by a correlating element;

a despreading element that operates via random access of buffers that are currently in read state to accumulate energy for a particular multi-path component;

a weighting element that weights the despread energy for a particular multi-path component using a channel estimate of the particular multi-path component; and

an accumulator that iteratively accumulates the despread energy for each particular multi-path component into a buffer.

8. The apparatus of claim 7, further comprising a power control operable to power-down circuitry after the processing of all desired multi-

path components and to power-up when the next buffer of sample data is ready to be processed.

9. The apparatus of claim 7, wherein there are three physically separate buffers such that at any given time, one of the three physically separate buffers is receiving data, and two of the three physically separate buffers comprise a logical buffer for random access by a correlator.

10. The apparatus of claim 7, wherein there are five physically separate buffers such that at any given time, two of the five physically separate buffers comprise a logically addressable space that is receiving data, and the other three of the five physically separate buffers comprise a logically addressable space for random access by a correlator.

11. The apparatus of claim 7, wherein the accumulator that iteratively accumulates the despread energy for each particular multi-path component into a buffer selectively locates the despread energy into an output memory buffer or an intermediate results buffer.

12. The apparatus of claim 7, further comprising circuitry to perform searches for multi-path components by correlating against a timing hypothesis.

13. The apparatus of claim 7, further comprising separate sets of physical buffers for even and odd digital samples followed by a permutation block capable of mapping to one set of the separate sets of physical buffers to the searching element and one set of the separate sets of physical buffers to the demodulation element, whereby the permutation

block manages contention between the searching element and the demodulation element for data in a same memory block.

14. The apparatus of claim 13, wherein the permutation block is selected by providing correct timing of digital samples to the demodulator, and by providing the searching element with the other set of digital samples.

15. The apparatus of claim 7, further comprising:

means for tuning to a non-original RF frequency;

means for buffering digital samples obtained while tuned at the non-original RF frequency;

means for retuning the RF frequency to the original frequency; and

means for performing searching and channel estimation via the random access of the digital samples stored in the first memory element while simultaneously operating on the digital samples of the original frequency.

16. The apparatus of claim 15, wherein the means for buffering digital samples obtained while tuned at the non-original RF frequency maintains digital samples from the non-original RF frequency after retuning the RF frequency to the original frequency.

17. The apparatus of claim 7, further comprising means for processing a plurality of sets of digital samples from a plurality of distinct receiver RF chains.

18. The apparatus of claim 7, further comprising means for processing multi-path components corresponding to transmit diversity.

19. The apparatus of claim 7, further comprising means for dynamically switching to optimal functionality based on channel estimates.

20. A demodulator operable with spread spectrum signals in a multi-path communication environment, the demodulator comprising:

a despreader that obtains digital samples from a first memory buffer by randomly accessing the first memory buffer, whereby the despreader is adaptable to arbitrary sample rates and symbol times;

a channel estimator that obtains digital sample information from the despreader and provides a channel estimate of a particular multi-path component; and

an accumulator that accumulates the digital samples from the despreader into a second memory buffer based on the channel estimate from the channel estimator.

21. The demodulator of claim 20, wherein an algorithm used to accumulate the digital samples into the second memory buffer is selected dynamically via the channel estimate.

22. The demodulator of claim 20, wherein the digital samples are randomly accessible from the first memory buffer.

23. The demodulator of claim 20, further comprising feedback in which data is read from the second memory buffer and used in the

accumulation of the digital samples from the despreader into the second memory buffer.

24. The demodulator of claim 20, wherein the accumulated digital samples comprise partially processed symbols.

25. The demodulator of claim 20, further comprising a power controller configured to toggle between an off state and an on state.

26. The demodulator of claim 20, wherein the digital samples obtained from the first memory buffer include a burst-pilot signal that is time-division multiplexed, wherein the burst-pilot signal includes information relating to a cellular channel used to determine the channel estimate.

27. The demodulator of claim 20, wherein the digital samples obtained from the first memory buffer include a continuous-pilot signal, wherein the continuous-pilot signal includes information relating to a cellular channel used to determine the channel estimate.

28. The demodulator of claim 20, wherein the digital samples obtained from the first memory buffer include signals communicated in a multiple transmit, multiple receive antenna scheme.

29. The demodulator of claim 20, wherein the accumulator that accumulates the digital samples from the despreader selectively locates the digital samples into the second memory buffer or an intermediate results buffer.